

**BIDIRECTIONAL
ESD PROTECTION DIODES**

STAND-OFF VOLTAGE - **12.0** Volts
POWER DISSIPATION - **350** WATTS

GENERAL DESCRIPTION

- Electro Static Discharge (ESD) protection diodes in ultra small SMD Plastic packages designed to protect one signal line from the damage caused by ESD and other transients.

FEATURES

- Bidirectional ESD protection of one line.
- Max. peak pulse power : Ppp = 350W at tp = 8/20 us
- ESD protection >25KV per MIL-STD-883C, Method 3015-6:Class3
- IEC 61000-4-2, level 4 (ESD), >15KV (air) ; >8KV (contact).

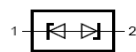
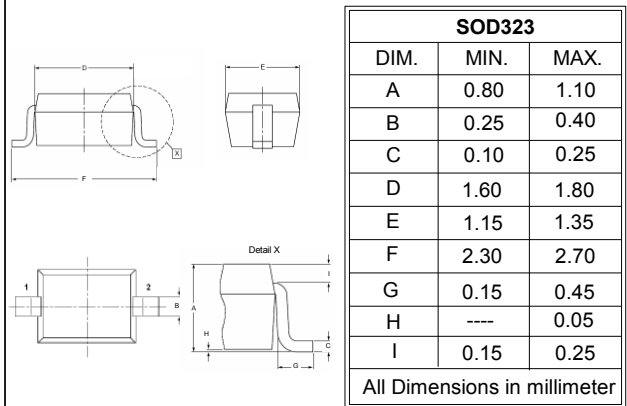
APPLICATION

- Computers and peripherals
- Communication system
- Notebooks. Desktops & Servers.
- Portable electronics
- Cellular handsets and accessories.

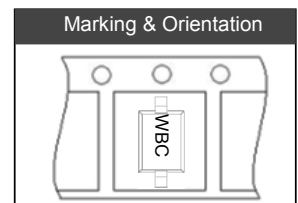
MECHANICAL DATA

- Case Material: "Green" molding compound UL flammability classification 94V-0 (No Br,Sb, Cl)
- Terminals: Lead Free Plating (Matte Tin Finish)
- Component in accordance to RoHs 2002/95/EC

SOD323



PIN ASSIGNMENT	
1	Cathode
2	Cathode



MAXIMUM RATINGS (Tj= 25°C unless otherwise noticed)

Rating	Symbol	Value	Unit
Peak pulse Power (8/20us Waveform)	PPPM	350	W
Peak Pulse Current (8/20us Waveform)	I _{PP}	15	A
Operating Junction Temperature Range	T _J	-55 to + 150	°C
Storage Temperature Range	T _{stg}	-55 to + 150	°C
Soldering Temperature, t max = 10s	T _L	260	°C

ELECTRICAL CHARACTERISTICS (Tj= 25°C unless otherwise noticed)

Parameter	Symbol	Conditions	Min	Max	Unit
Reverse standoff voltage	V _{DRM}	---	---	12.0	V
Reverse leakage current	I _{RM}	V _{DRM} = 12 V	---	1	uA
Breakdown voltage	V _{BR}	I _R = 1 mA	13.3	15.5	V
Diode capacitance	C _J	V _R = 0 V , f = 1MHz	---	100	pF
Clamping voltage	V _{CL}	I _{PP} = 15A (8/20us)	---	24	V

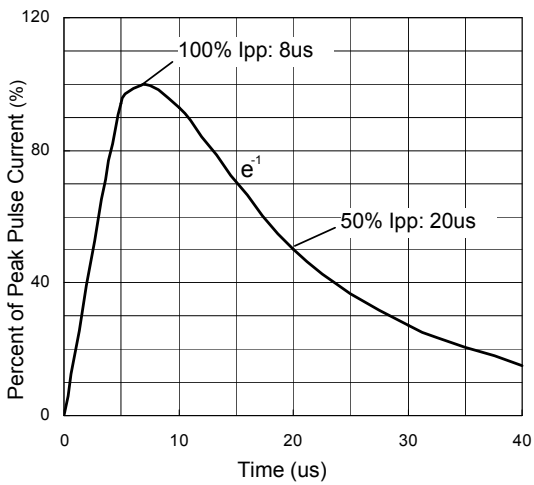


Figure 1. 8/20 us pulse waveform according to IEC 61000-4-5

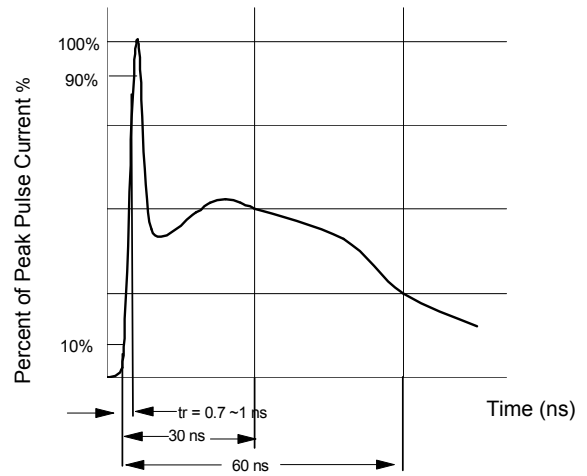


Figure 2. ESD pulse waveform according to IEC 61000-4-2

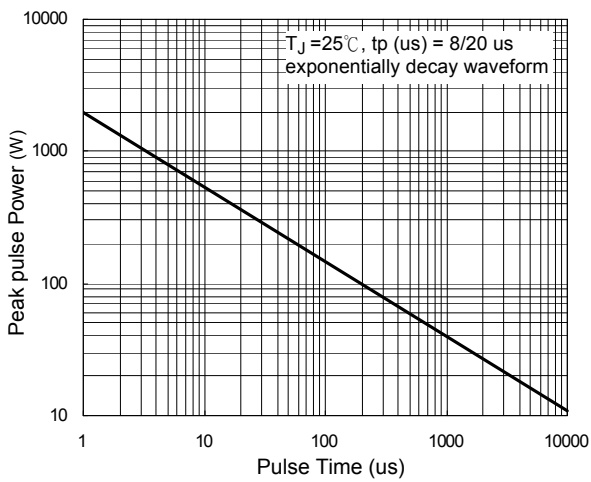


Figure 3. Power Dissipation versus Pulse Time

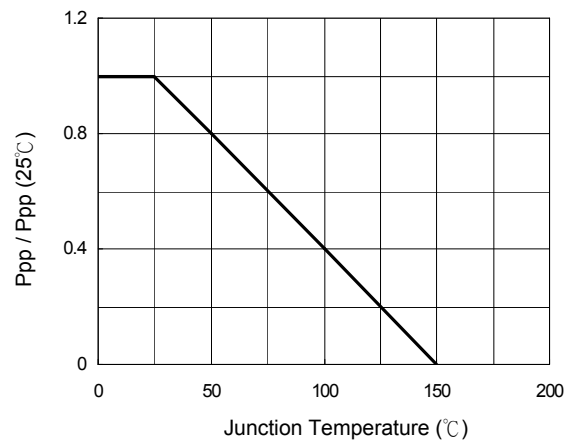


Figure 4. Peak pulse power versus TJ

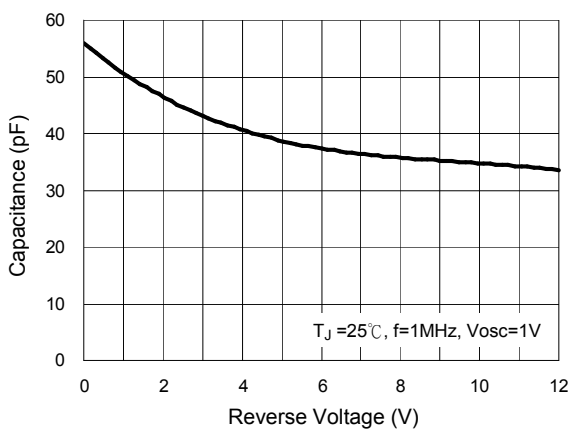


Figure 5. Typical Junction Capacitance

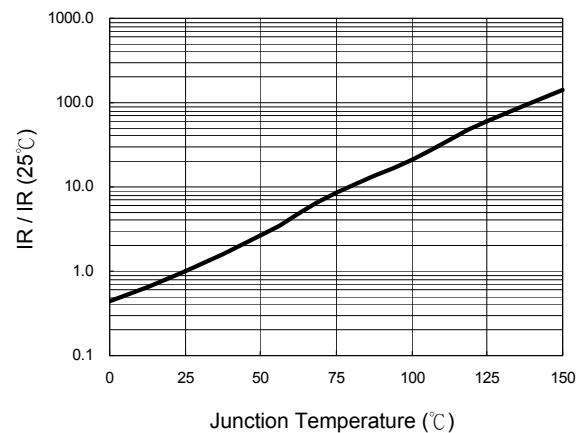


Figure 6. Reverse Leakage Current versus TJ

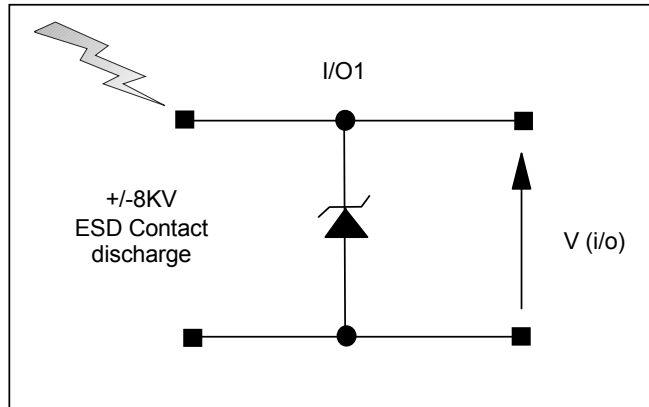


Figure 7. ESD Test Configuration

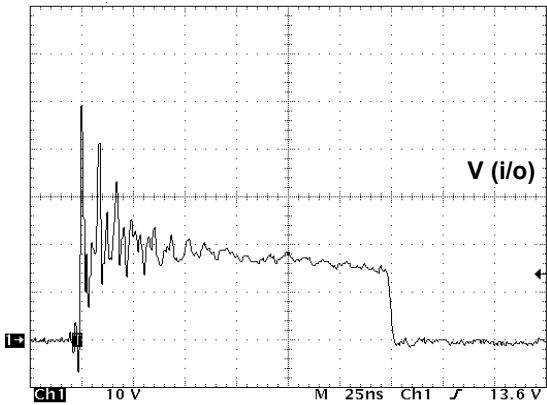


Figure 8. Clamped +8 kV ESD voltage waveform

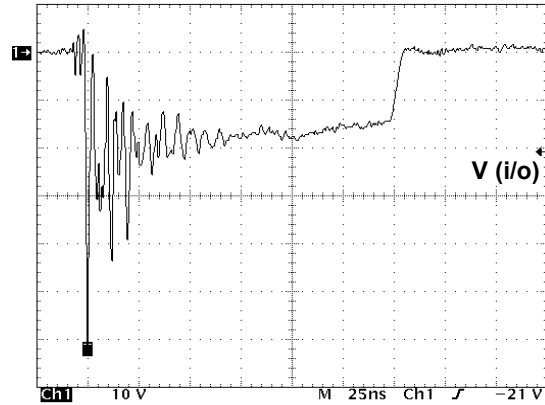


Figure 9. Clamped -8 kV ESD voltage waveform